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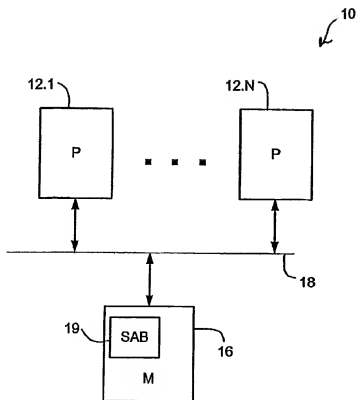
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[Continued on next page]

(54) Title: DECOUPLED STORE ADDRESS AND DATA IN A MULTIPROCESSOR SYSTEM



(57) Abstract: In a computer system having a plurality of processors connected to a shared memory, a system and method of decoupling an address from write data in a store to the shared memory. A write request address is generated for a memory write, wherein the write request address points to a memory location in shared memory. A write request is issued to the shared memory, wherein the write request includes the write request address. The write request address is noted in the shared memory and addresses in subsequent load and store requests are compared in share memory to the write request address. The write data is transferred to the shared memory and matched, within the shared memory, to the write request address. The write data is then stored into the shared memory as a function of the write request address.



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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ABTS D ET AL: "o many states, so little time: verifying memory coherehnce in the Cray X1" PARALLEL AND DISTRIBUTED PROCESSING SYMPOSIUM, 2003. PROCEEDINGS. INTERNATIONAL APRIL 22-26, 2003, PISCATAWAY, NJ, USA, IEEE, 22 April 2003 (2003-04-22), pages 11-20, XP010645295 ISBN: 0-7695-1926-1 pages 3-4	1-38
A	HENNESSY J L, PATTERSON D A: "Computer Architecture. A quantative approach" June 2002 (2002-06), MORGAN KAUFMANN, XP002318184 pages 390-423	1-38

☐ Further documents are listed in the continuation of box C.

☐ Patent family members are listed in annex.

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